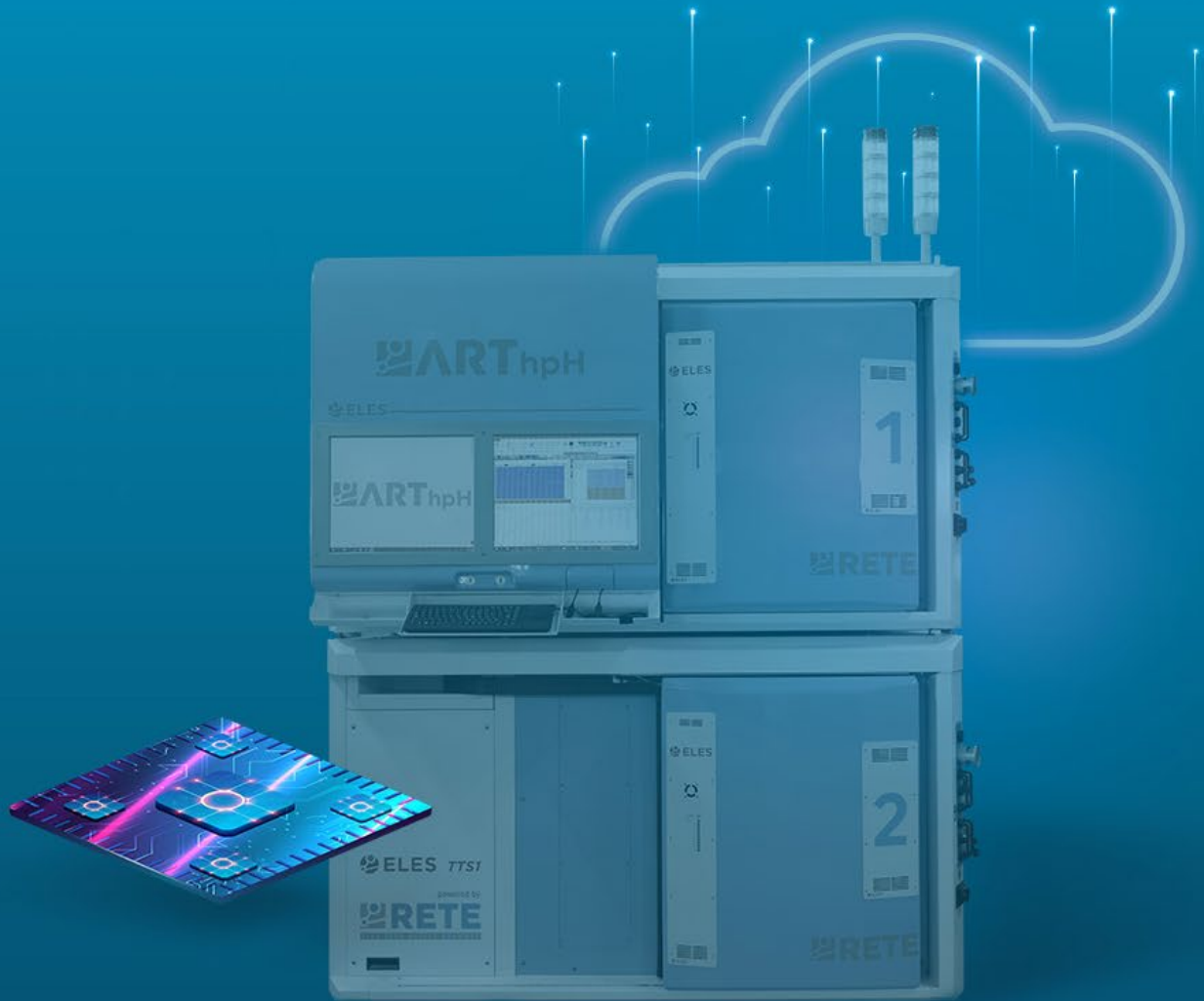




White Paper

Using Deep Data Analytics to Enhance Reliability Testing

The fast roadmap for Zero Defects by
proteanTecs & ELES

Abstract

Reliability testing relies on industry-standard test methodologies such as JEDEC JESD47 and JESD22¹. Traditionally, System On Chip (SOC) devices are assembled on special boards and placed in the oven for accelerated lifetime stress, running unmonitored test patterns such as Automatic Test Pattern Generation (ATPG) and Memory Built-In Self-Test (MBIST), and are typically tested using normal test techniques outside the oven, at specified times (e.g., 48, 168, 500 and 1000 hours for standard High Temperature Operating Life (HTOL) acceleration at 125°C).

More advanced reliability test equipment, such as ELES ART5xx², in combination with proper IC Design setup for Reliability Test (DfRT) allows running more complex test sequences and checking their response in-situ, during the in-oven stress time. The result is an effective stress test, able to trigger and detect design and process weakness (TfR – Test for Reliability methodology).

The reliability challenges of modern automotive and mission critical applications require going beyond the classical ways to perform IC reliability test. They require the use of innovative approaches to guarantee the application of the adequate stress vs. Mission Profile, to measure performance degradation more precisely and with fine granularity, simplifying the search for root cause analysis (RCA) and enabling an effective design and manufacturing process improvement for Zero Defects.

This paper will explore the benefits and improvements that can be achieved by using deep data extracted from in-chip monitors when coupled with test equipment that is capable of running interactive tests and connected to data analytics software.

1. Stress-Test-Driven Qualification Of Integrated Circuits | JEDEC_
2. Innovative reliability tests | Todi, PG | ELES S.p.A.

1 | Introduction

Reliability testing assumes that when a device is toggling, under high temperature and voltage, it will be exposed to a stress equivalent of what it would face during its intended lifetime, by applying an Acceleration Factor (AF) formula.

The normal JEDEC defined HTOL test procedure will include:

- Randomly selecting 77 units from each of three different/subsequent lots
- Verifying all units using the complete Final Test (FT) patterns
- Running structural testing patterns (e.g., ATPG, MBIST) in loop under stress for 48 hours (“burn-in” or Dynamic Voltage Stress (DVS)
- Repeating (2)
- Continuing the same stress-verify sequence at 168 hours, 500 hours and 1000 hours observation points
- The test is considered as pass if after the last verification, none of the devices experienced a test failure, but even one failed device means the entire test flow must be repeated

It is evident that if an outlier device (a device that may contain a latent defect or manufactured outside the allowed process window) is used for the test and failed prematurely, the entire test was invalid and needs to be repeated, wasting a lot of money and time (1000 hours is nearly 1.5 months!). It will also be very difficult to pinpoint a failure and provide sufficient data for accurate root cause analysis (RCA). In addition, even if the test eventually passed, there is no quantitative data on the amount of degradation and how much margin-to-fail is still left.

Another critical aspect is that having stress and measurement in different test insertions may affect results. Possible stress recovery effects after stress removal could affect the off-oven measurements itself, leading to imprecise assessment of performance degradation. Stress and test must go together.

In Automotive applications for example, a device is intended to function at an extended lifetime, sometimes up to 15 years. At the same time, it is not assumed that the device will operate at 100% stress all the time. Instead, a Mission Profile is defined capturing the required budget of temperature, voltage, and activity factor, for a certain percentage of the operating lifetime. An important requirement is that HTOL will match that Mission Profile as much as possible.

Experience tells us that quite often, the test environment itself is responsible for failures due to wrong temperature and voltage calibration, other sensitive components on the board, or over-stress/under-stress test patterns used while in the oven. All these contribute to reduced confidence in the HTOL as a predictor for actual life expectancy of the device.

In the rest of this document, we will describe the proteanTecs Performance and Health Monitoring (PHM) system and how it can be used to help selection of the units to be tested, detecting and predicting early failures, quantifying the aging, validating the mission profile, reducing setup errors and providing data useful information for RCA, leading to overall cost reduction and improved confidence.

The paper will also describe the main benefits of PHM coupled with ELES ART Reliability test platform and TfR methodology in terms of reliability test flow automation, aging measurement and avoidance of inaccuracies caused by stress recovery effects.

2 | proteanTecs In-Chip Monitoring

proteanTecs Performance and Health in-chip monitoring solution is comprised of monitoring IPs, called Agents, that are designed into the IC and measure vital performance indicators during test or in normal operation mode. proteanTecs data analytics software is deployed at the Cloud or on the Edge (e.g., on the Automated Test Equipment, or ATE) to analyze the data and provide insights about how the IC is performing during its operation.

3 | ELES ART5xx and TfR Methodology

ELES ART5xx adaptive reliability test platform allows to combine the application of accelerated stress and test together in the same equipment (TfR) during qualification trials, leveraging Reliability Test oriented IC testability (DfRT).

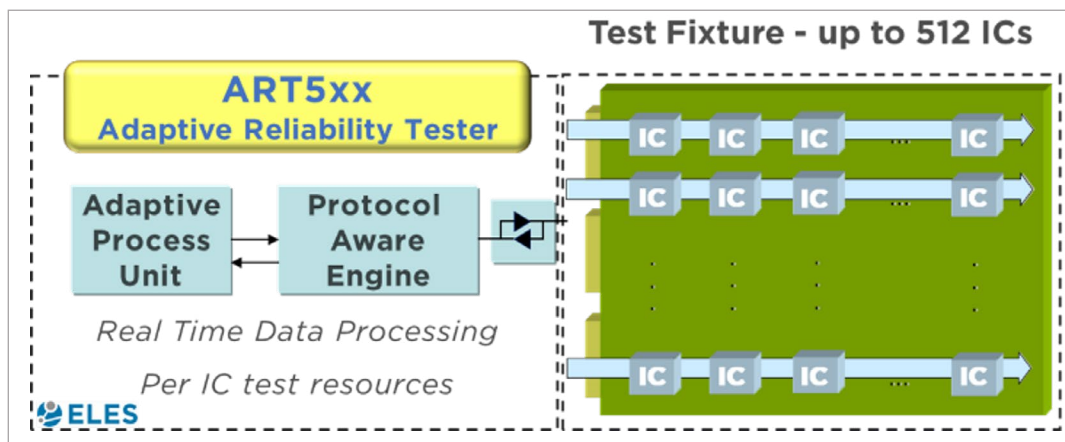


Figure 1: ART5xx: DfT Adaptive Tester

The evaluation of the device behavior, performance and degradation during the application of stress conditions is continuously captured and analyzed by RTI SW (Real Time Interpreter) in parallel for the entire qualification lot. Enhancement in terms of reliability measurements is possible by integrating embedded on-die feedback from the proteanTecs Agents into the TfR flow.

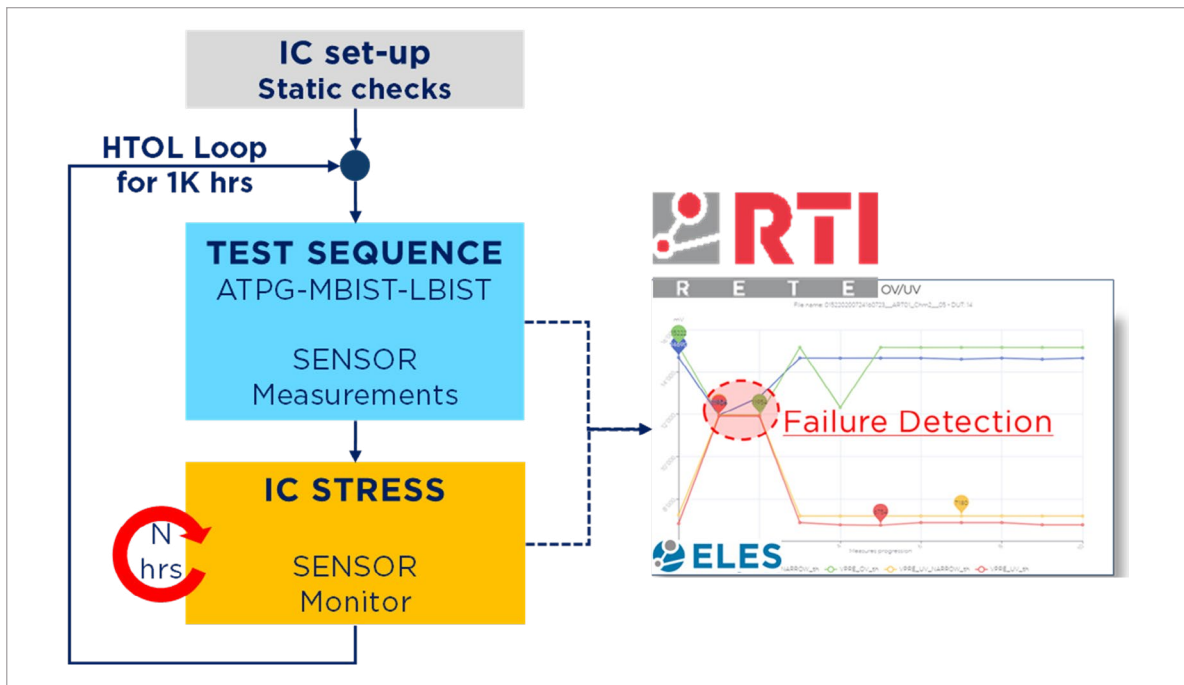


Figure 2: TfR – HTOL Test & Stress in the same flow for SOC ICs

The main benefits of TfR flow enriched by Agent measurements are:

- Full and real time control of applied stress vs. Mission Profile, in combination with relevant Agent measurements
- Possibility to apply adaptive stress/test strategies based on Agent feedback
- Performance measurements with fine granularity going beyond standard checkpoints on ATE
- Avoiding stress recovery effects due to separate stress and test phases
- Qualification experiment automatization, eliminating the need to move parts between different equipment, saving weeks compared to the standard process

Data collected during TfR flow, empowered by Agents feedback, are fundamental to improve Design and manufacturing process enabling an effective Learn from fail towards Zero Defects.

4 | Smart Material Selection

Data collected during TfR flow, empowered by Agents feedback, are fundamental to improve Design and manufacturing process enabling an effective Learn from fail towards Zero Defects.

The standard operating procedure for selecting devices to be HTOL tested according to JEDEC, calls for random selection of 77 devices from 3 consecutive lots. In practice, they are selected from 3 corner lots with the assumption that this will provide full coverage for the process manufacturing range. This is no longer sufficient as the parametric variation is too wide in advanced process nodes.

We propose a new method of selecting the samples that will represent the widest parametric variation from each of these lots. It is based on proteanTecs Classification and Profiling Agents that map each area in the chip to its representative manufacturing parameters based on the simulated Process Design Kit (PDK). This creates a high resolution “Die Fingerprint” for each area in each die on the wafer, as can be seen in **Figure 3**, and algorithms running on the cloud to find those with the widest parametric distribution.

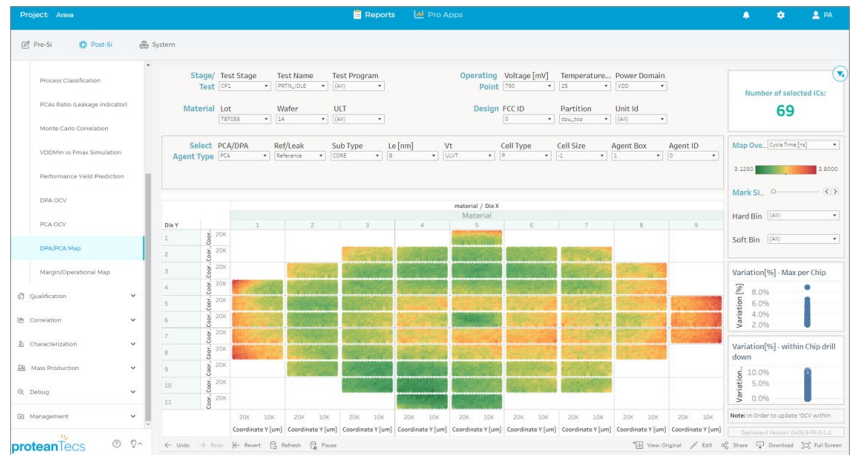


Figure 3: Die fingerprinting using ML-driven deep data

In **Figure 4**, we see an example of selection of 77 units (marked in blue) out of available 2,757 (orange) from one lot, that were chosen to provide the widest parametric coverage of the PDK.

Additional benefit of using proteanTecs Smart Material Selection is that it will flag and screen units that fall outside of the allowed process window, thereby reducing the risk of failure due

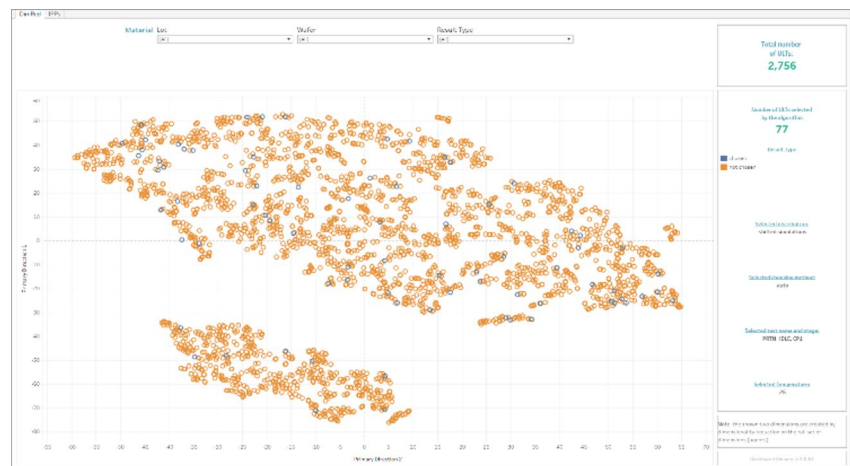


Figure 4: Smart Material Selection in the cloud

5 | Monitoring and Outlier Detection

While in the oven and running structural or functional test patterns, proteanTecs Classification and Profiling Agents will continue to monitor the parametric variation of each of the transistor types and representative cells used in the design.

This can be seen in the following image, **Figure 5**:

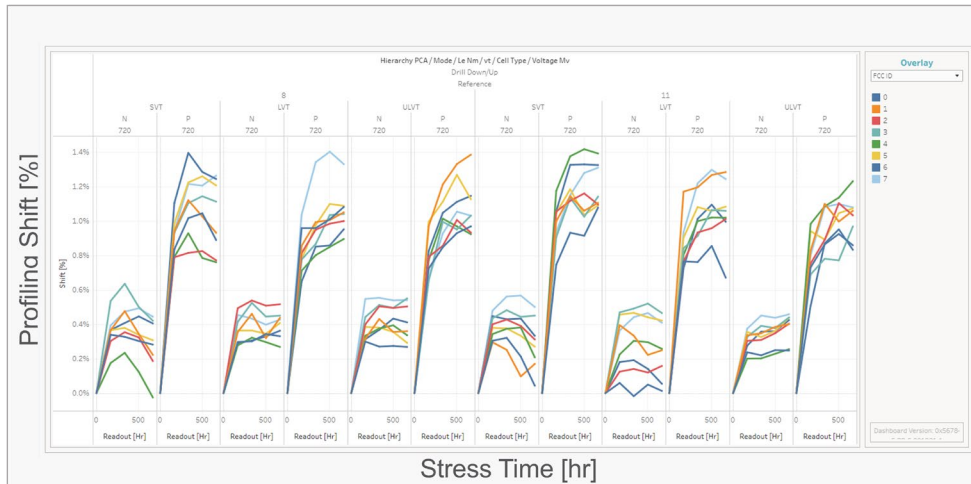


Figure 5: Degradation per transistor type

In addition, proteanTecs Performance and Degradation Monitoring Agents are used to continuously track the remaining timing to the target clock frequency at very high coverage, and by monitoring these margins over time, we can track and visualize the degradation effects in each small section of the design and predict time to failure.

In **Figure 6**, we can see degradation monitoring of actual logic by measuring remaining timing margins to the target clock. As can be observed, one logic area in the design, the lowest one, shown in purple, is degrading faster than the rest and is likely to fail before the 500 hours readout point. If this behavior is seen on all samples, this is a good indication of an overstressed area in the chip, or a design sensitivity.

If, however, only one unit is showing such a behavior, it may indicate a latent defect and it may be preferable to stop the test and restart with a fresh set of units, rather than spend more time just to get a functional test failure in the end.

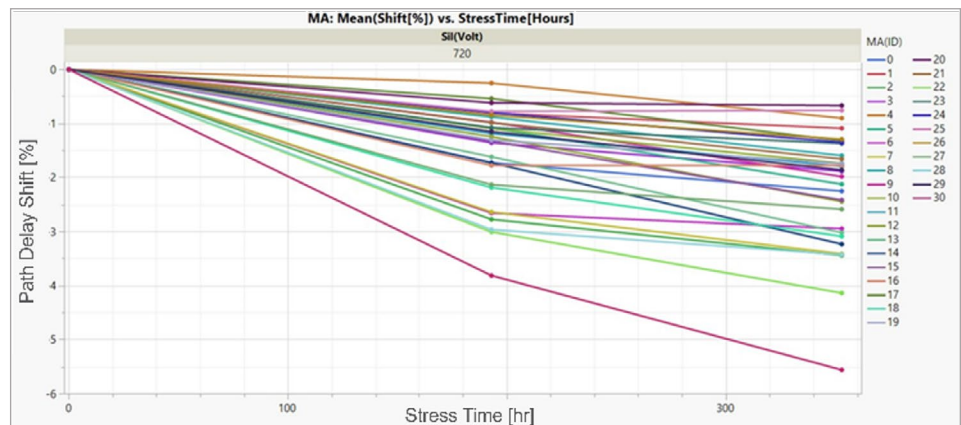


Figure 6: Timing degradation monitoring

For holistic real-time, continuous monitoring of the degradation of each Device Under Test (DUT) while in the Reliability Test platform, proteanTecs on-tester software application visualizes the temperature, voltage, stress and worst timing margin over time. That information is applied on a Reliability Function and Time to Failure is calculated, as can be seen in **Figure 7** below.

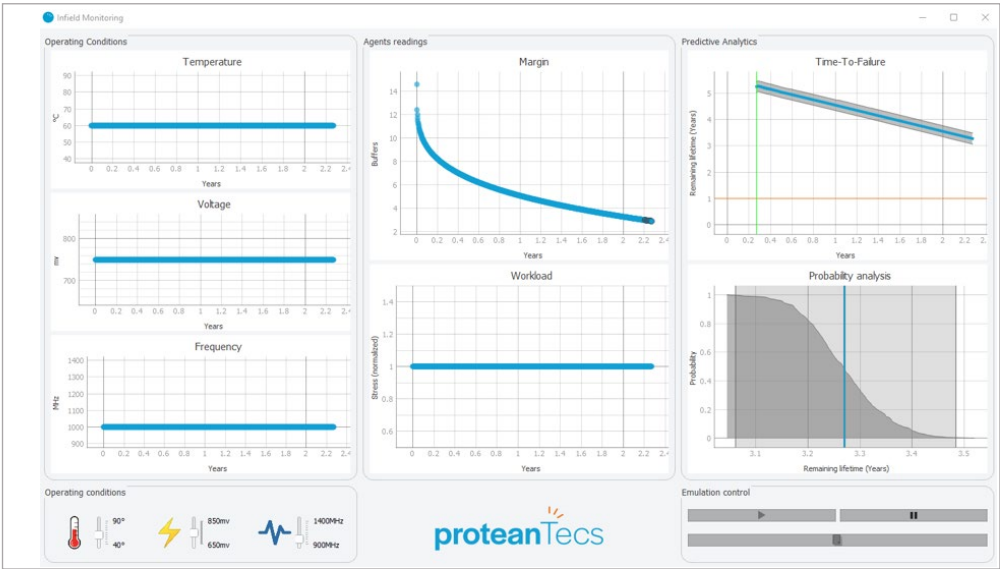


Figure 7: Real time degradation monitoring

6 | Mission Profile Validation

Automotive semiconductors are designed with Mission Profile in mind, which represents the amount of stress the device is expected to experience throughout its lifetime. The stress is represented by a combination of voltage, temperature and activity rate for a certain percentage of the device lifetime. proteanTecs Workload Agents, can continuously measure that stress and feed the information to verify an equivalent stress was applied during the HTOL test. **Figure 8** shows how the Mission Profile is converted to the expected reading of the different Workload Agents.

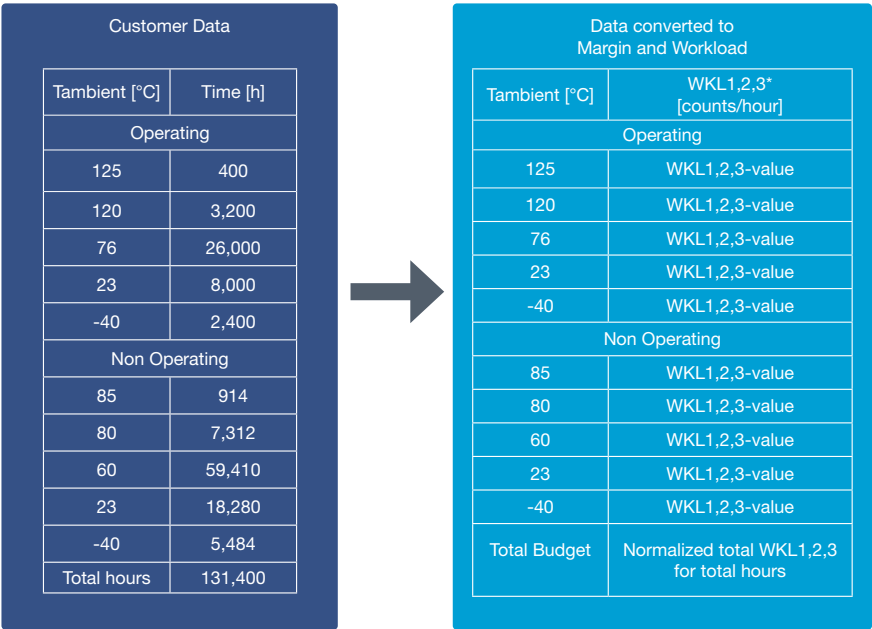


Figure 8: Mission Profile data conversion to Margins and Workloads

In **Figure 9**, we demonstrate an application running on the HTOL tester (or on an edge device) to monitor the Mission Profile budget consumption during the stress test. The Mission Profile is monitored via the Workload Agents during the test and is fed to the application where it is converted back to the Mission Profile. In addition, the application will display in real time, the measured voltage, temperature, frequency and worst-case timing margins, to predict remaining time to consume the Mission Profile budget.

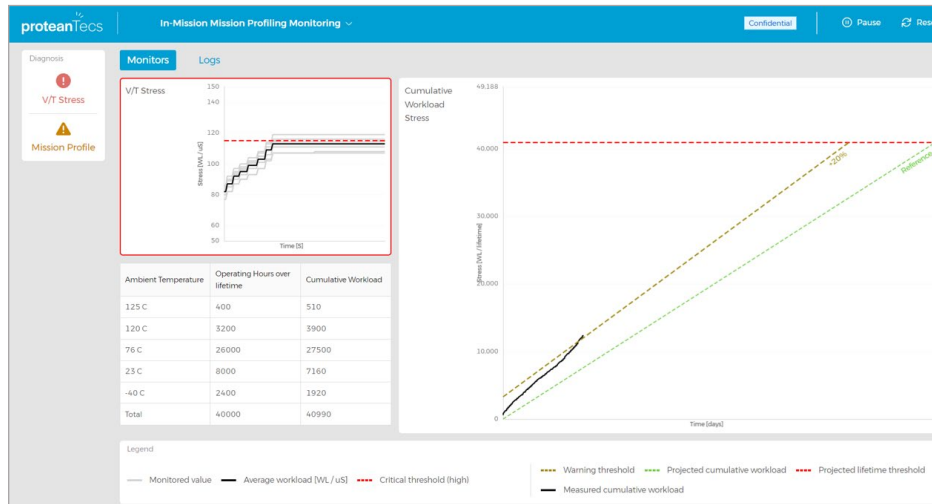


Figure 9: Mission profile validation and Workloads

ART Platform, thanks to its adaptive stress and test capabilities can read Workload Agents feedback from the software at the edge and adjust in real time the relevant stress matrix in order to better match Mission Profile and trial duration targets.

7 | Burn-In with Confidence, Environment Validation and RCA

An underlying assumption for the reliability of the HTOL test is a correct and uniform setting of voltages and temperatures in the oven. This is typically achieved by using sensors on the load board.

The example (**Figure 10**), shows an early alert of a non-uniform degradation that was observed, and had triggered a root cause analysis with the customer. In this example, two boards are shown, BIB 2 and BIB 10. BIB 2 shows a normal distribution of the degradation as the higher degraders (red) are randomly distributed. On the other hand, BIB 10 shows a very distinctive pattern that that “lower” half is degrading more than the “upper” half.

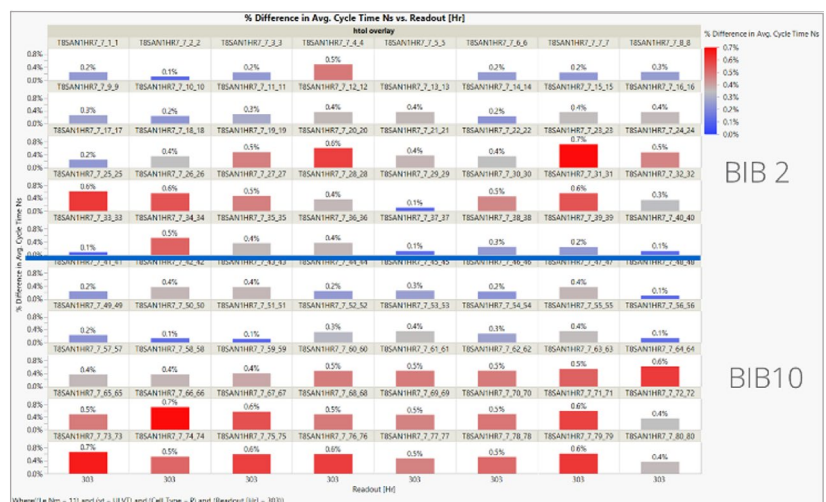


Figure 10: Degradation anomaly detection

The proteanTecs Local Voltage and Temperature Sensors were used to extract accurate measurements from within the DUTs, for improved accuracy and higher distribution. The Data Analytics Platform was used to generate a spatial image out of these readings for easy and early identification of wrong voltage or temperature settings, or unintended gradient across the DUTs.

Such a visualization is shown in **Figure 11**, showing correlation of lower-than-expected degradation, to lower temperature on the “upper” half of the board.

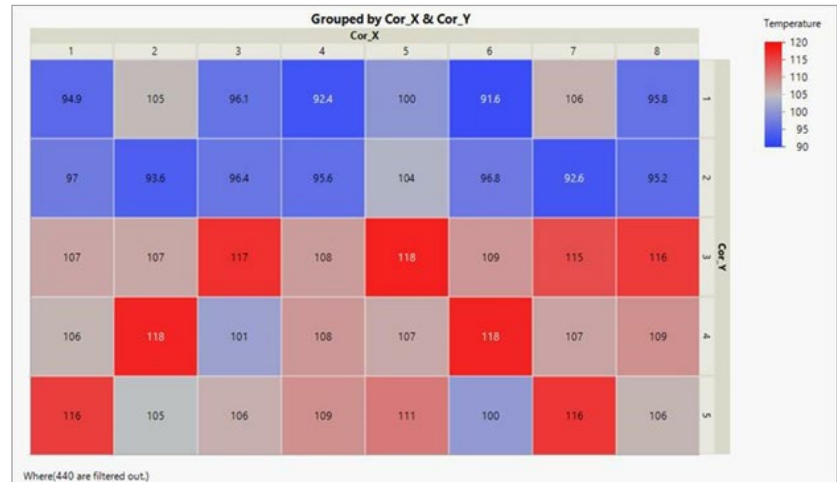


Figure 11: Board thermal map (BIB10)

8 | Conclusions

Applying Smart Material selection for Reliability Test, using deep data extracted from the DUT during reliability testing while the DUT is still under stress (TfR), combined with advanced analytics on the Cloud, Edge Client on the ART Reliability tester, will guarantee proper stress level during the qualification trials vs Mission Profile targets and the detection of relevant ICs failures/anomalies/performance degradation, fundamental for the Learn for Fail process. This will add significant confidence, improve reliability towards zero defects, shorten time to RCA, and lower cost and risk to customers.



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